

Software Variability from the Nomadic Devices Perspective

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- Micro-Electronics research organization located Leuven, Belgium
 - Mission “To perform R&D, ahead of industrial needs by 3 to 10 years, in microelectronics, nanotechnology, design methods and technologies for ICT systems”
- Numbers
 - Budget: ± 200 M€
 - Staff: ± 1700
 - Cleanroom: ± 10,000 m²



Nomadic Devices

Nomadic Devices



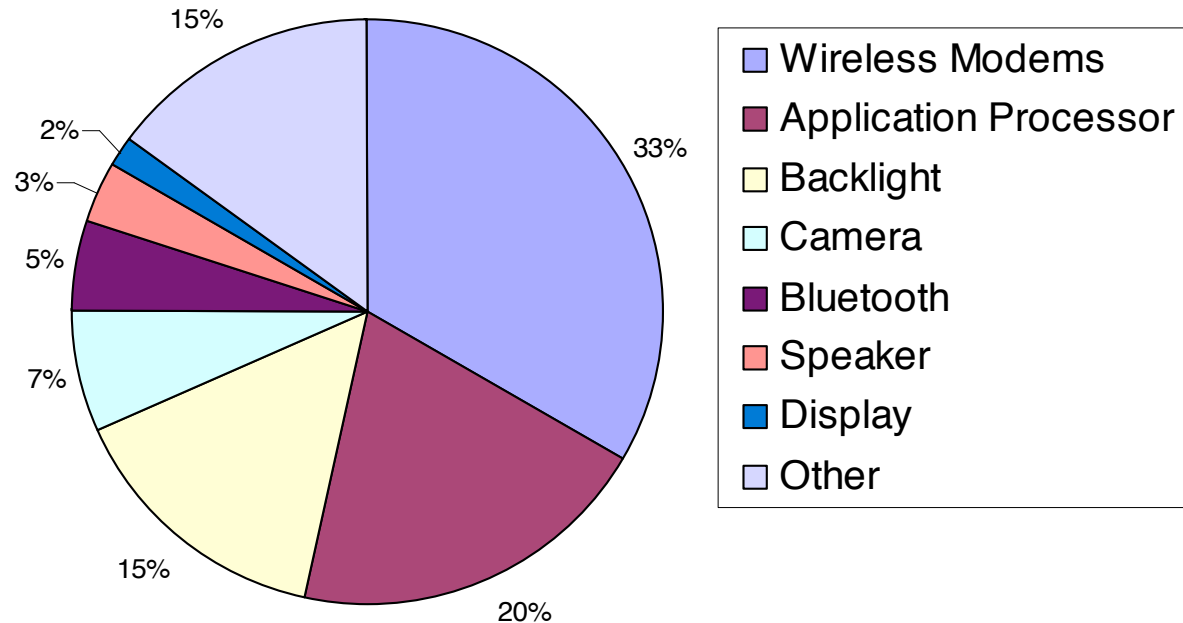
Nomadic Device Characteristics

- Power and energy constraints (battery)
- Design time constraints (time to market)
- Cost
- Real-time constraints
- Flexibility and performance



Handheld Battery-powered Devices

3W

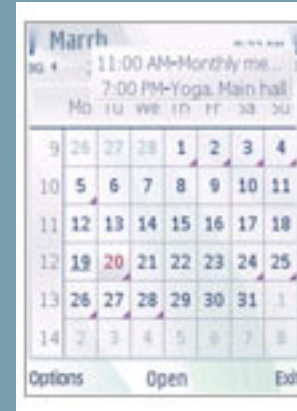
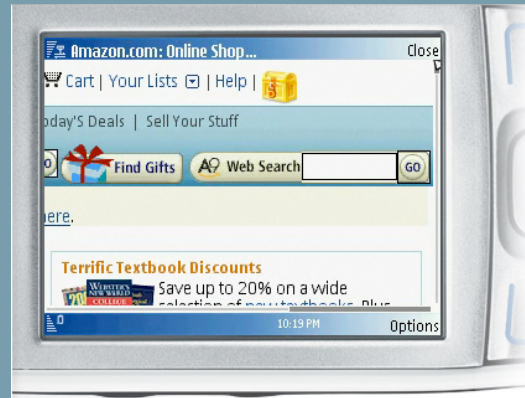
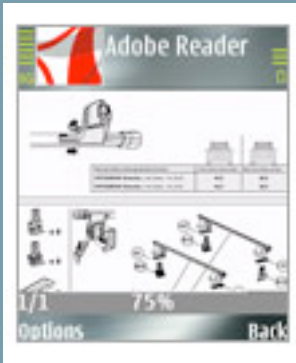


- ➔ Max 1.5W for processing
- ➔ Max 1W for SMP cores

[Yrjö Neuvo. Cellular phones as embedded systems. In Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC, volume 1, pages 32–37, February 2004.]

[Kimmo Kuusilinna, Nokia, Date'08]

Current Market

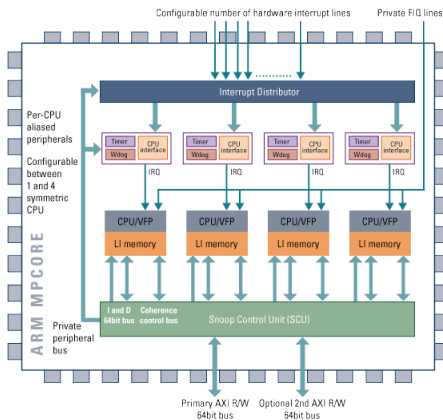


Concrete Numbers for the Belgian market

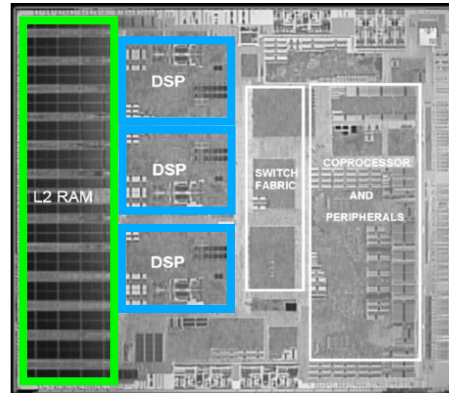
- Motorola: 21 models, 66 models in support
- Nokia: 94 models, 144 models in support
- Samsung: 34 models, 174 models in support
- LG: 18 models

Multicore is here to stay

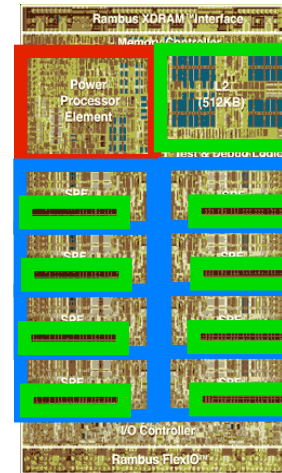
ARM



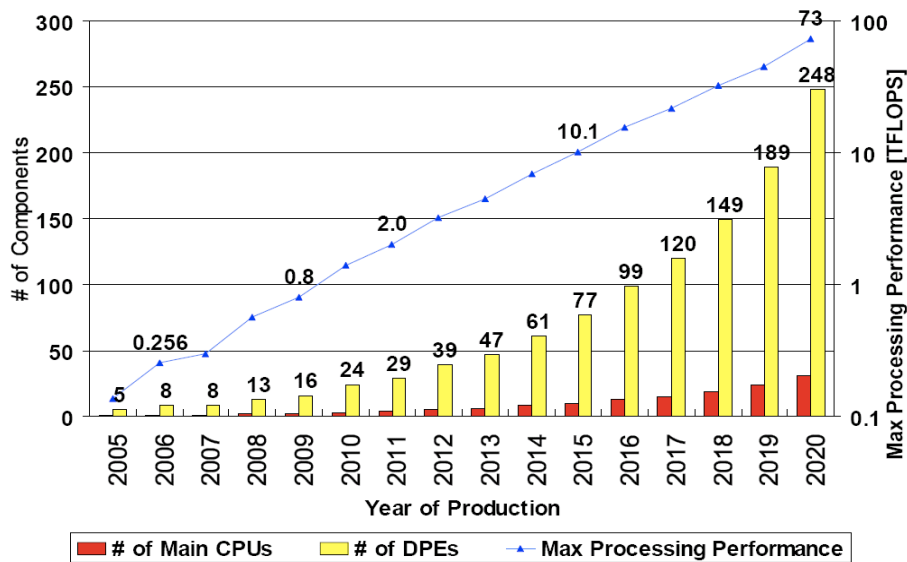
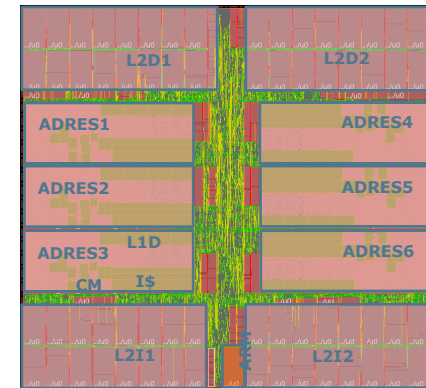
Texas Instruments



IBM Cell



IMEC



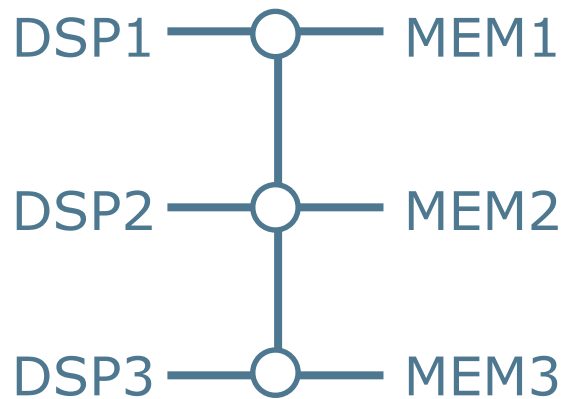
The key question:

“How to efficiently program them?”

Programming Nomadic Devices



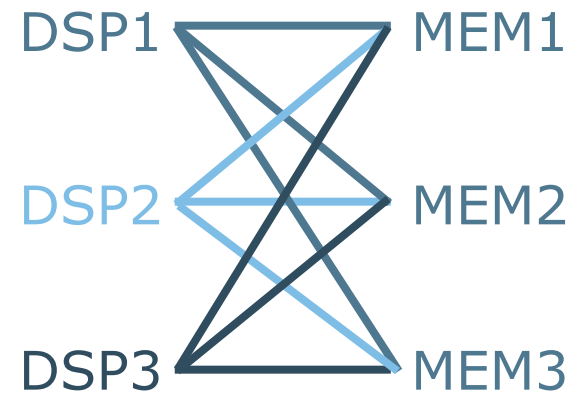
Design variability: example



DSP1 — MEM1

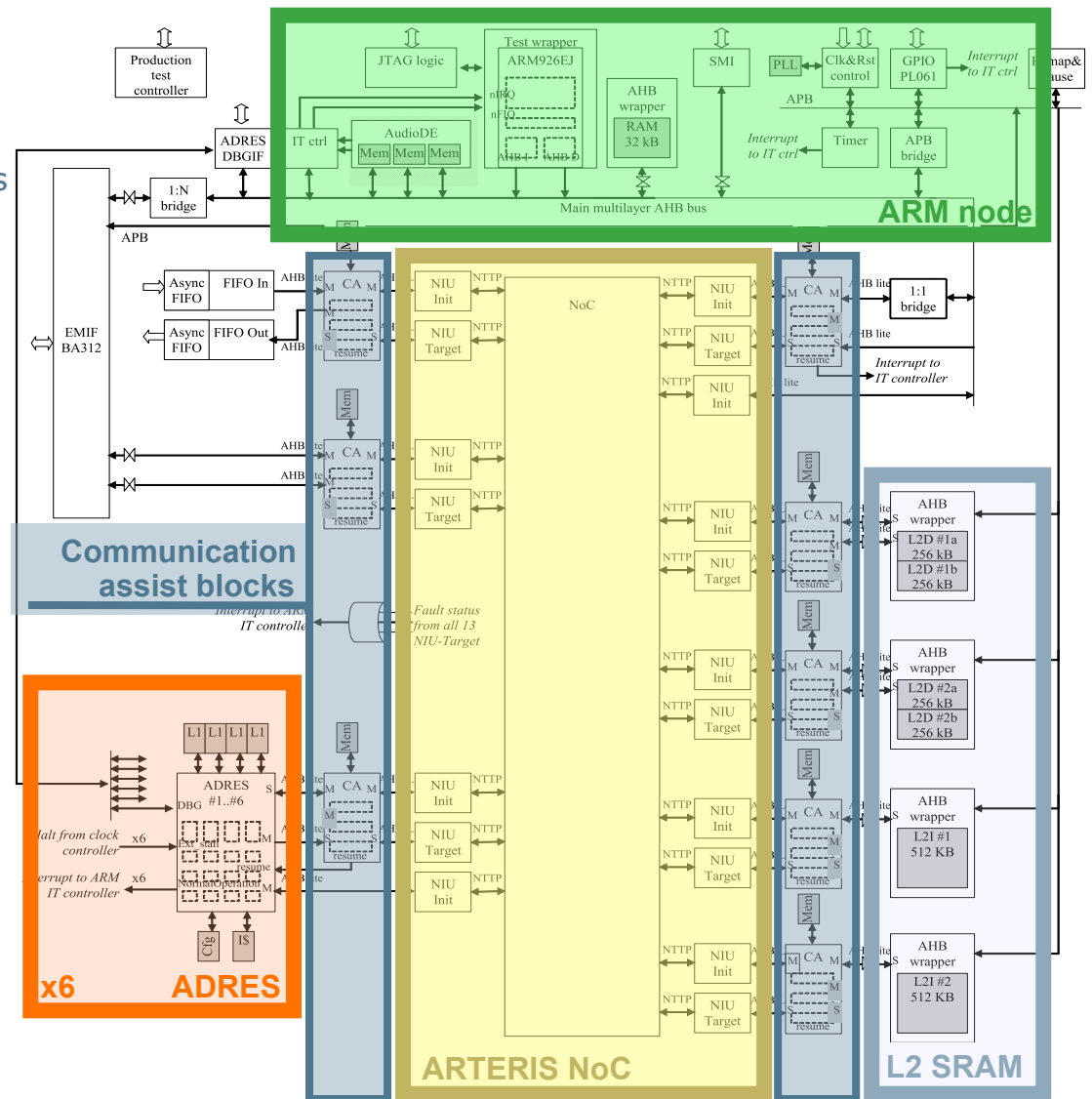
DSP2 — MEM2

DSP3 — MEM3

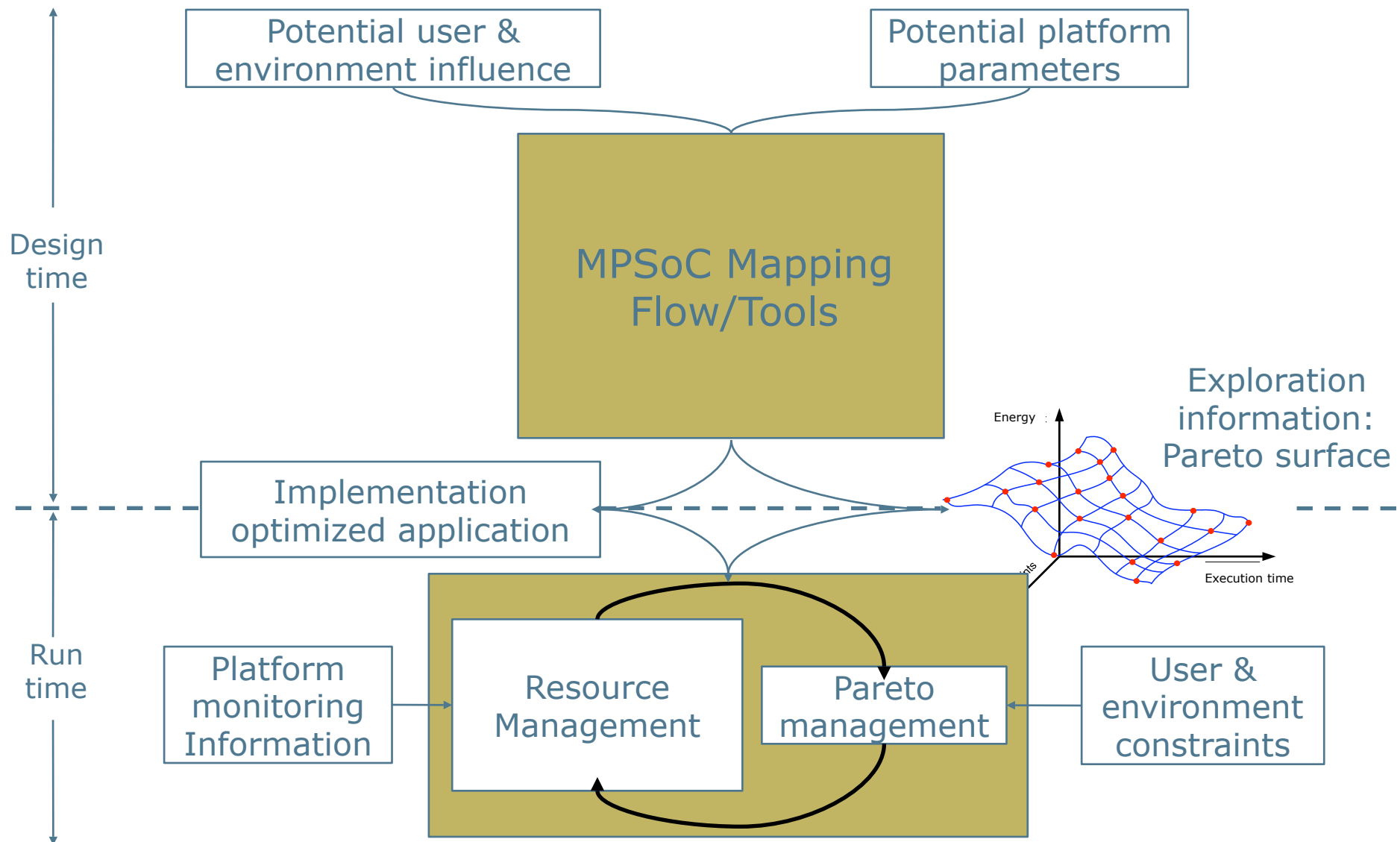


Design Variability: MPSoC Example

- 6 ADRES processors
 - 4x4 array, 3-issue VLIW
 - 32-bit datapath
 - 16 video CODEC specific instructions
 - 8 FUs with multipliers
 - Performance: 300MHz
- 13 Communication assist
 - Performance: 75/150MHz
- ARTERIS NoC
 - Separate instr. and data NoC
 - Bandwidth: 5Gbps@150MHz
- ARM926
 - System control
 - Performance: 75MHz
- L2 memory
 - L2I: 2 banks of 512kB
 - L2D: 4 banks of 256kB
- Voltage islands
 - ADRES processors
 - L2I and L2D banks
- Multiple clock domains



Dealing with variability: IMEC's Approach



Solution for MPSoC: IMEC MPA Tool

Parallelization directives

```

#pragma omp parallel
#pragma omp single
#pragma omp taskwait
#pragma omp taskwait

#pragma omp taskwait
#pragma omp taskwait
#pragma omp taskwait

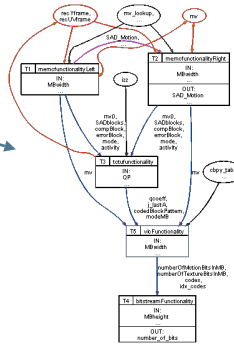
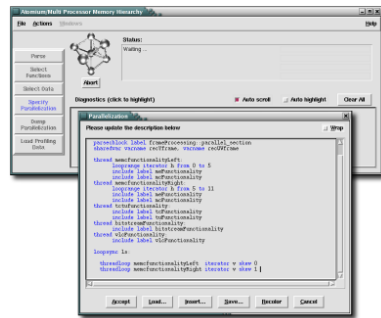
#pragma omp taskwait
#pragma omp taskwait
#pragma omp taskwait

#pragma omp taskwait
#pragma omp taskwait
#pragma omp taskwait
    
```

Application code

```

// Application code snippet
// ...
    
```



✓ Parallelizes sequential Clean-C source code

- ✓ *Correct-by-construction multi-threaded code*
- ✓ Higher level than OpenMP
- ✓ Directives in separate file

✓ Supported types of parallelism

- ✓ Functional split
- ✓ (Coarse) Data-level split
- ✓ Combinations

✓ Dumps parallel code

✓ Sets up communication

- ✓ Communication by means of FIFO's
- ✓ DMA transfers
- ✓ FIFO sizes determined by tool (initial version)

thread 1

thread 2

thread n

```

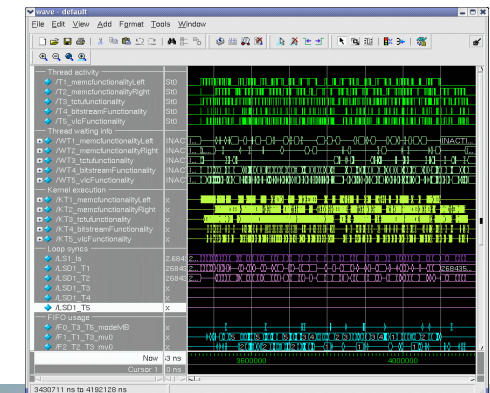
// Thread 1 code
// ...
    
```

```

// Thread 2 code
// ...
    
```

```

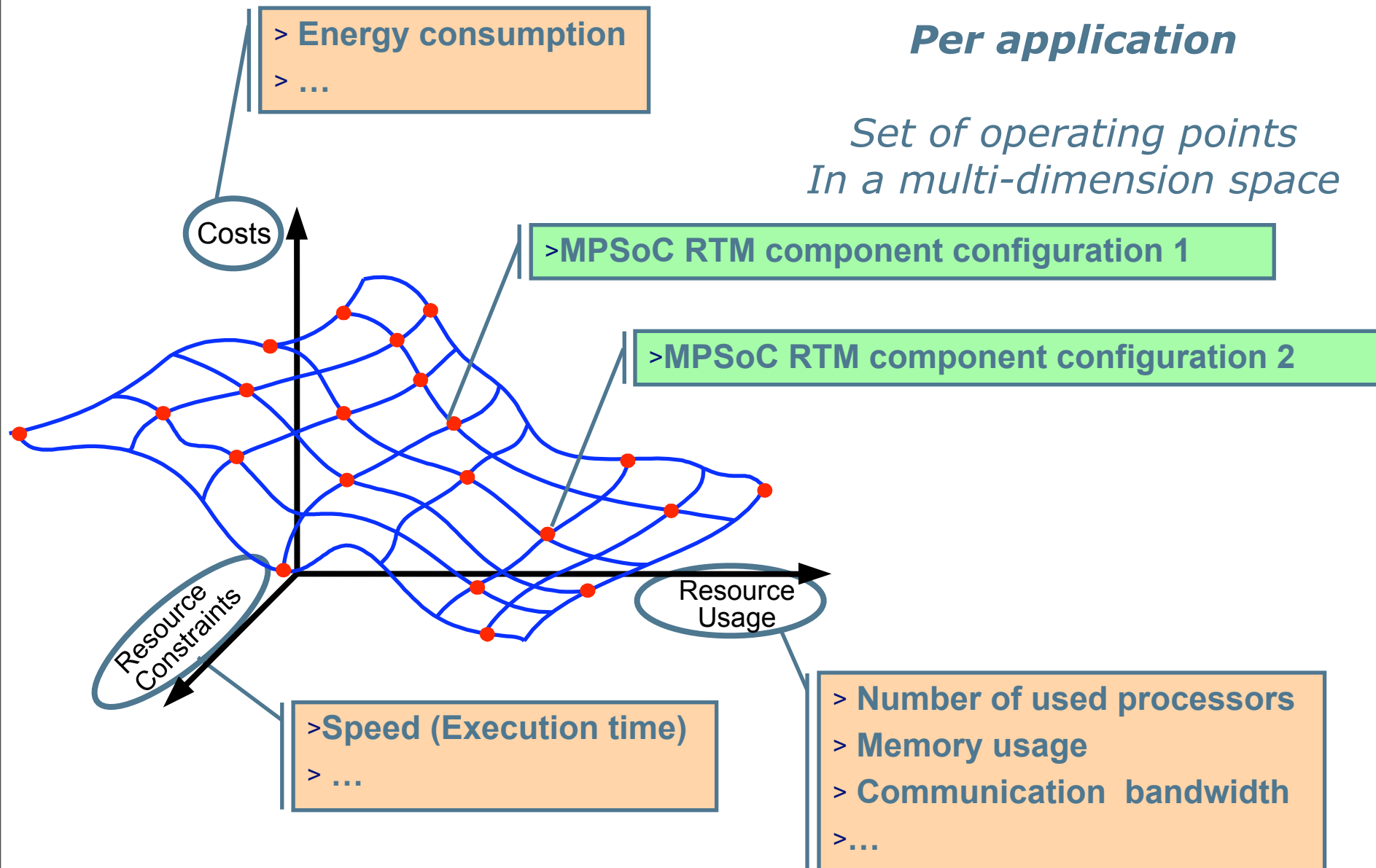
// Thread n code
// ...
    
```



Design Time Exploration

Per application

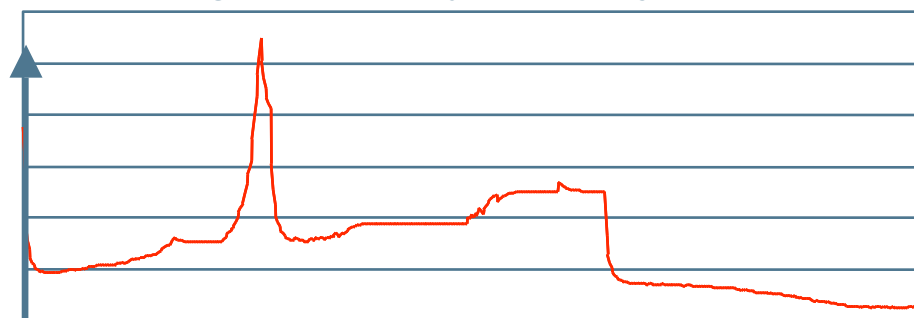
*Set of operating points
In a multi-dimension space*



Run-time management

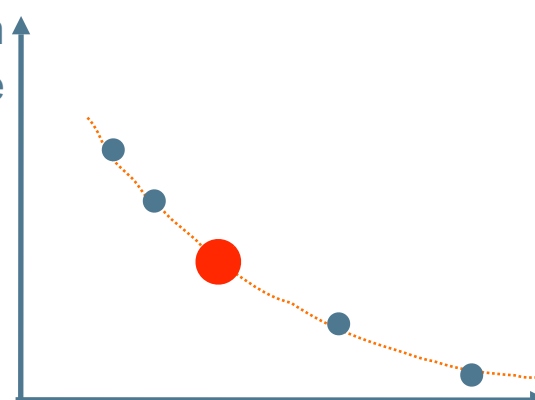
- For each thread frame, run-time scheduler changes management **dynamically** according to the run-time situations

Workload (e.g., complexity of 3D object rendered)



Time

Execution time

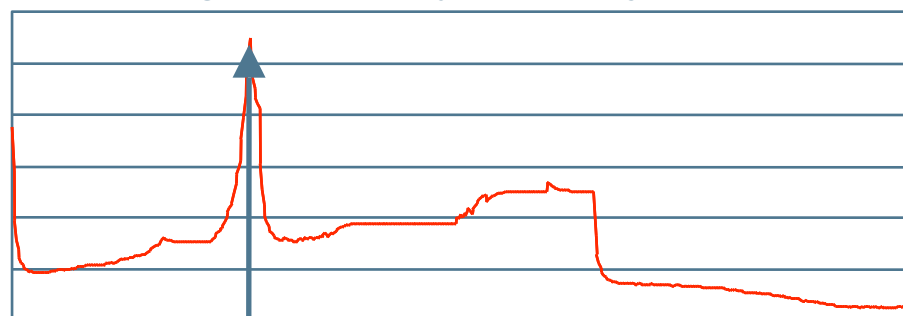


Power consumption

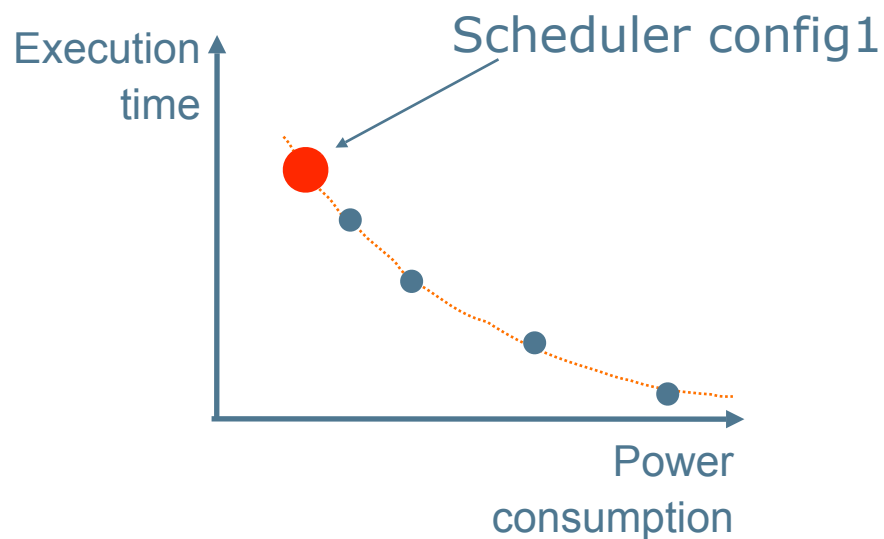
Run-time management

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Workload (e.g., complexity of 3D object rendered)



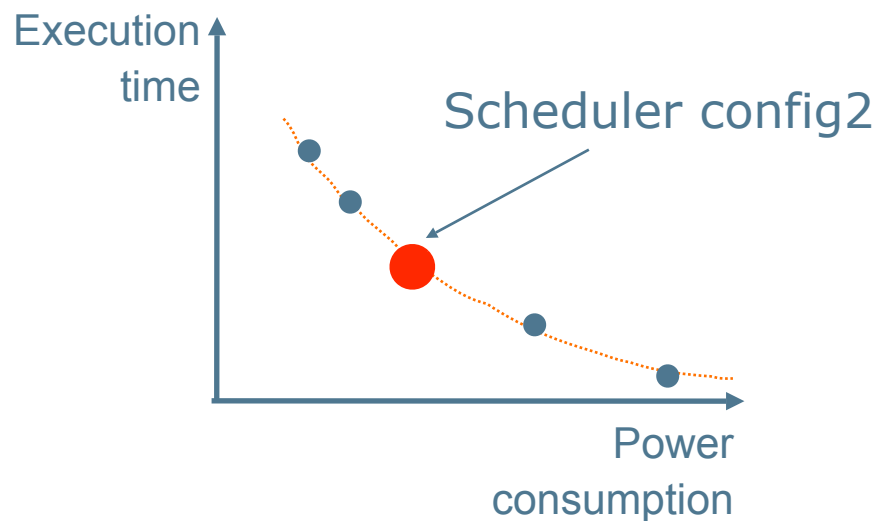
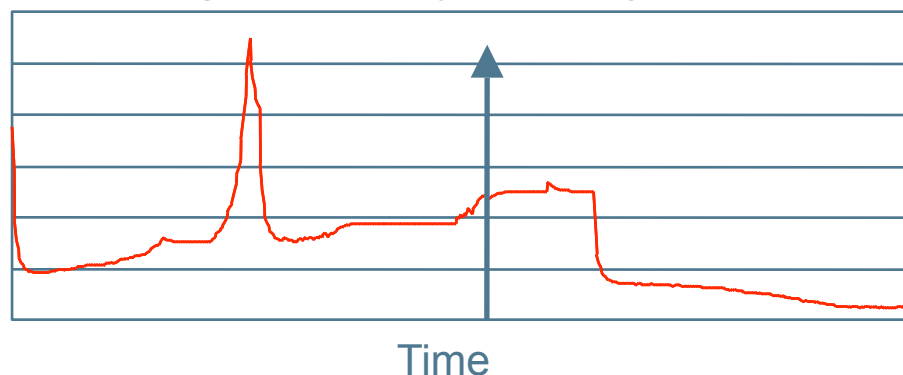
Time



Run-time management

- For each thread frame, run-time scheduler changes management **dynamically** according to the run-time situations

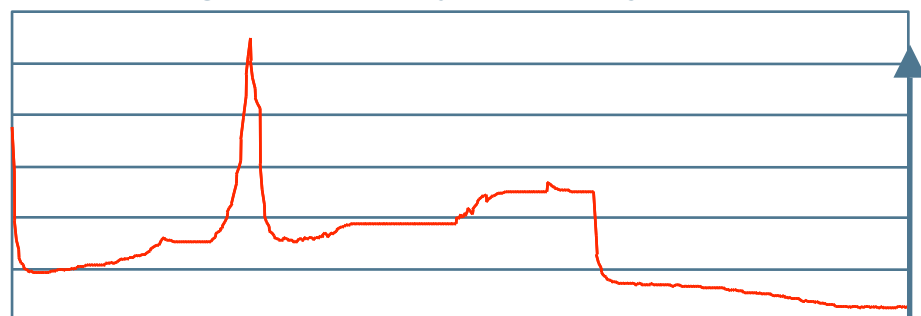
Workload (e.g., complexity of 3D object rendered)



Run-time management

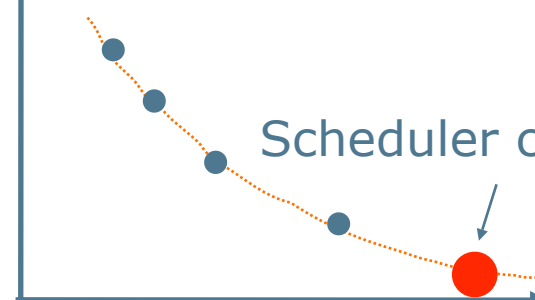
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Workload (e.g., complexity of 3D object rendered)



Time

Execution time



Scheduler config3

Power consumption

Recapitulation

- Requirements: energy conservation, real-time constraints, time to market
- Issues tackled:
 - Map source code to hardware
 - Optimized code for various scenarios
 - Switch between scenarios at runtime
- Issues not tackled:
 - Huge design time effort
 - Applications are becoming more and more dynamic
 - Closed world assumption lifted: loading and unloading of new applications

Food for thought: Upcoming Issues

- **Not too distant future:**
 - Manycore chips
 - 3D chips
 - Chip Variability
 - Chip Unreliability
- **Further away:**
 - Biological Computing

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